## CLAIMS

What is claimed is:

1. A predistortion circuit for compensating linear distortion introduced by analog-transmitter components of a digital communications transmitter, said predistortion circuit comprising:

a source of a complex-forward-data stream configured to digitally convey information;

a digital equalizer section coupled to said complex-forward-data-stream source and configured to generate an equalized-complex-forward-data stream and to pass said equalized-complex-forward-data stream to said analog-transmitter components;

a feedback section adapted to receive a feedback signal from said analog-transmitter components and configured to provide a complex-return-data stream; and

a controller coupled to said feedback section and to said equalizer section and configured so that said equalizer section compensates for frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components.

2. A predistortion circuit as claimed in claim 1 wherein said analog-transmitter components include a power amplifier having an input and an output, and said feedback section comprises:

a first analog input adapted to receive a first RF-analog signal from said power amplifier input; and

a second analog input adapted to receive a second RF-analog signal from said power amplifier output.

3. A predistortion circuit as claimed in claim 2 wherein said controller is configured to compensate for linear distortion in an RF-analog signal present at said input of said power amplifier, then compensate for linear distortion in an amplified RF signal present at said output of said power amplifier.

4. A predistortion circuit as claimed in claim 1 wherein said equalizer section comprises:

a non-adaptive equalizer configured to be programmed with filter coefficients; and

an adaptation engine coupled to said non-adaptive equalizer and configured to implement an estimation-and-convergence algorithm which determines said filter coefficients.

5. A predistortion circuit as claimed in claim 4 wherein said non-adaptive equalizer processes said complex-forward-data stream, and said adaptation engine is responsive to said complex-forward-data stream and said complex-return-data stream.

6. A predistortion circuit as claimed in claim 4 wherein:

said non-adaptive equalizer is a complex equalizer having an in-phase path, a quadrature path, an in-phase-to-quadrature path, and a quadrature-to-in-phase path;

a first set of said filter coefficients is programmed in said in-phase and quadrature paths, and a second set of said filter coefficients is programmed in said in-phase-to-quadrature and quadrature-to-in-phase paths; and

said adaptation engine accommodates a partial complex equalizer and has first and second paths, said first and second

paths being configured in one mode to determine said filter coefficients for said in-phase and quadrature paths, and being configured in another mode to determine said filter coefficients for said in-phase-to-quadrature and quadrature-to-in-phase paths.

7. A predistortion circuit as claimed in claim 1 wherein said equalizer section implements an estimation-and-convergence algorithm to determine filter coefficients that compensate for said frequency dependent quadrature gain and phase imbalance.

8. A predistortion circuit as claimed in claim 7 wherein:

said estimation-and-convergence algorithm is responsive to said complex-forward-data stream and to said complex-return-data stream;

said complex-forward-data stream and said complex-return-data stream exhibit forward-error and return-error levels, respectively, with said return-error level being greater than said forward-error level; and

said estimation-and-convergence algorithm is configured to transform increased algorithmic processing time into reduced effective-error level for said complex-return-data stream.

9. A predistortion circuit as claimed in claim 7 wherein said estimation-and-convergence algorithm causes said equalizer section to converge at said filter coefficients after processing a multiplicity of samples from said complex-return-data stream.

10. A predistortion circuit as claimed in claim 7 wherein said

said estimation-and-convergence algorithm is responsive to said complex-forward-data stream and to said complex-return-data stream;

said complex-forward-data stream and said complex-return-data stream exhibit a forward-error level and a return-error level, respectively, with said return-error level being greater than said forward-error level; and

said estimation-and-convergence algorithm controls a rate of convergence upon said filter coefficients to achieve a predetermined effective return-error level that is less than said return-error level.

11. A predistortion circuit as claimed in claim 1 wherein said equalizer section implements a complex equalizer.

12. A predistortion circuit as claimed in claim 1 wherein:

said complex-forward-data stream exhibits a forward resolution; and

said complex-return-data stream exhibits a return resolution less than said forward resolution.

13. A predistortion circuit as claimed in claim 12 wherein said feedback section generates said complex-return-data stream so that said return resolution is at most four bits less than said forward resolution.

14. A predistortion circuit as claimed in claim 1 wherein said feedback section comprises a complex-digital-subharmonic-sampling downconverter adapted to receive said feedback signal from said analog-transmitter components and configured to provide said complex-return-data stream.

15. A predistortion circuit as claimed in claim 1 additionally comprising a programmable delay element coupled between said complex-forward-data-stream source and said feedback section, said programmable delay element being configured to produce a delayed-complex-forward-data stream temporally aligned with said complex-return-data stream.

16. A predistortion circuit as claimed in claim 15 wherein:

said complex-forward-data stream propagates through said predistortion circuit in response to a clock signal; and

said programmable delay element includes an integral section that delays at least a portion of said complex-forward-data stream by an integral number of cycles of said clock signal and includes a fractional section that delays said portion of said complex-forward-data stream by a fraction of a cycle of said clock signal.

17. A predistortion circuit as claimed in claim 15 wherein:

said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element and to said feedback section and having an output coupled to said controller; and

said controller and said correlator are configured to implement an estimation-and-convergence algorithm to bring said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream.

18. A predistortion circuit as claimed in claim 15 wherein said controller is configured to cause said

programmable delay element to temporally align said delayed-complex-forward-data stream with said complex-return-data stream prior to causing said equalizer section to compensate for said frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components.

19. A predistortion circuit as claimed in claim 15 wherein:

said equalizer section comprises an adaptive equalizer configured to determine filter coefficients that compensate for said frequency dependent quadrature gain and phase imbalance; and

said adaptive equalizer increases correlation between said delayed-complex-forward-data stream and said complex-return-data stream in determining said filter coefficients.

20. A predistortion circuit as claimed in claim 1 wherein:

said analog-transmitter components include a band-pass filter which inserts a band-pass-filter delay; and

said predistortion circuit additionally comprises a phase rotator configured to rotate one of said complex-forward-data and complex-return-data streams relative to the other to compensate for said band-pass-filter delay.

21. A predistortion circuit as claimed in claim 20 wherein said phase rotator is configured to implement an estimation-and-convergence algorithm to determine an amount of phase rotation that compensates for said band-pass-filter delay.

22. A predistortion circuit as claimed in claim 20 wherein said controller is configured to cause said phase rotator to compensate for said band-pass-filter delay prior to causing said equalizer section to compensate for said frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components.

23. A predistortion circuit as claimed in claim 20 wherein:

said equalizer section comprises an adaptive equalizer configured to determine filter coefficients that compensate for said frequency dependent quadrature gain and phase imbalance; and

said adaptive equalizer increases correlation between said complex-forward-data and complex-return-data streams after rotation of one of said complex-forward-data and complex-return-data streams relative to the other in determining said filter coefficients.

24. A predistortion circuit as claimed in claim 1 wherein said equalizer section includes a first equalizer configured to filter said complex-forward-data stream and a second equalizer configured to filter said complex-return-data stream.

25. A predistortion circuit as claimed in claim 24 wherein:

said first equalizer is a non-adaptive equalizer programmed with forward-filter coefficients;

said second equalizer is a non-adaptive equalizer programmed with return-filter coefficients; and

said equalizer section additionally includes an adaptation engine selectively coupled to said first and second equalizers

and configured to implement an estimation-and-convergence algorithm which determines said forward-filter and return-filter coefficients.

26. A predistortion circuit as claimed in claim 24 wherein:

said analog-transmitter components include a power amplifier having an input and an output;

said feedback section has a first analog input adapted to receive a first RF-analog signal from said power amplifier input and a second analog input adapted to receive a second RF-analog signal from said power amplifier output;

said controller is configured to cause said feedback section to monitor said first RF-analog signal while adjusting said first equalizer to compensate for linear distortion at said input of said power amplifier, then cause said feedback section to monitor said second RF-analog signal while further adjusting said first equalizer to compensate for linear distortion at said output of said power amplifier.

27. A predistortion circuit as claimed in claim 26 wherein said controller is configured to, after adjusting said first equalizer to compensate for linear distortion at said output of said power amplifier, monitor said second RF-analog signal while adjusting said second equalizer to further compensate for linear distortion at said output of said power amplifier.

28. A predistortion circuit as claimed in claim 27 wherein:

said first equalizer is adjusted to increase correlation between said second RF-analog signal and a first signal

responsive to said complex-forward-data stream and having a first bandwidth; and

said second equalizer is adjusted to increase correlation between said second RF-analog signal and a second signal responsive to said complex-forward-data stream and having a second bandwidth wider than said first bandwidth.

29. A predistortion circuit as claimed in claim 24 wherein:

said analog section includes a power amplifier which exhibits a gain; and

said predistortion circuit additionally comprises an adjustable attenuation circuit configured to compensate for said gain of said power amplifier and positioned to process said complex-return-data stream before filtering in said second equalizer.

30. A predistortion circuit for compensating linear distortion introduced by analog-transmitter components of a digital communications transmitter, said predistortion circuit comprising:

a source of a complex-forward-data stream configured to digitally convey information;

a quadrature-balance-adjustment section coupled to said complex-forward-data-stream source for providing a balanced-complex-forward-data stream and passing said balanced-complex-forward-data stream to said analog-transmitter components;

a digital-subharmonic-sampling downconverter adapted to receive a feedback signal from said analog-transmitter components and configured to provide a complex-return-data stream; and

a controller coupled to said downconverter and to said quadrature-balance-adjustment section and configured so that said quadrature-balance-adjustment section compensates for quadrature gain and phase imbalance introduced by said analog-transmitter components.

31. A predistortion circuit as claimed in claim 30 additionally comprising:

a local-oscillator-input port adapted to receive a local-oscillator signal from said analog-transmitter components, said local-oscillator signal exhibiting a local-oscillator frequency used by said analog-transmitter components for up-conversion;

a synthesizer circuit for synthesizing a clock signal exhibiting a frequency equal to said local-oscillator frequency times $2N\pm1$ divided by four, where N is a positive integer selected to satisfy the Nyquist criteria for a bandwidth within which linear distortion is to be compensated; and

wherein said digital-subharmonic-sampling downconverter includes an analog-to-digital converter configured to sample said feedback signal at a rate determined by said clock signal.

32. A predistortion circuit as claimed in claim 30 wherein:

said complex-forward-data stream exhibits a forward resolution; and

said complex-return-data stream exhibits a return resolution less than said forward resolution.

33. A predistortion circuit as claimed in claim 32 wherein said downconverter generates said complex-return-data stream so that said return resolution is at most four bits less than said forward resolution.

34. A predistortion circuit as claimed in claim 30 additionally comprising a programmable delay element coupled between said complex-forward-data-stream source and said downconverter, said programmable delay element being configured to produce a delayed-complex-forward-data stream, said delayed-complex-forward-data stream being temporally aligned with said complex-return-data stream.

35. A predistortion circuit as claimed in claim 34 wherein:

said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element and to said downconverter and having an output coupled to said controller; and

said controller and said correlator are configured to implement an estimation-and-convergence algorithm to bring said

delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream.

36. A predistortion circuit as claimed in claim 34 wherein:

said programmable delay element is a first programmable delay element that adjusts for common mode delay between said complex-return-data and complex-forward-data streams; and

said transmitter additionally comprises a second programmable delay element coupled between said complex-forward-data-stream source and said downconverter, said second programmable delay element being configured to adjust for differential mode delay.

37. A predistortion circuit as claimed in claim 34 wherein:

said complex-forward-data stream propagates through said predistortion circuit in response to a clock signal; and

said programmable delay element includes an integral section that delays at least a portion of said complex-forward-data stream by an integral number of cycles of said clock signal and includes a fractional section that delays said portion of said complex-forward-data stream by a fraction of a cycle of said clock signal.

38. A predistortion circuit for compensating linear distortion introduced by analog-transmitter components of a digital communications transmitter, said predistortion circuit comprising:

a source of a complex-forward-data stream configured to digitally convey information;

a quadrature-balance-adjustment section coupled to said complex-forward-data-stream source for providing a balanced-complex-forward-data stream to said analog-transmitter components;

a feedback section adapted to receive a feedback signal from said analog-transmitter components and to generate a complex-return-data stream; and

a controller coupled to said feedback section and to said quadrature-balance-adjustment section and configured to implement one or more estimation-and-convergence algorithms in processing said complex-return-data stream to adjust said quadrature-balance-adjustment section to compensate for said linear distortion introduced by analog-transmitter components.

39. A predistortion circuit as claimed in claim 38 wherein:

said complex-forward-data stream exhibits a forward resolution; and

said complex-return-data stream exhibits a return resolution less than said forward resolution.

40. A predistortion circuit as claimed in claim 39 wherein said feedback section generates said complex-return-data stream so that said return resolution is at most four bits less than said forward resolution.

41. A predistortion circuit as claimed in claim 38 wherein:

said quadrature-balance-adjustment section includes an adaptive equalizer; and

said controller is configured to implement an estimation-and-convergence algorithm through said adaptive equalizer, wherein said estimation-and-convergence algorithm of said adaptive equalizer converges upon filter coefficients which cause said quadrature-balance-adjustment section to compensate for said linear distortion introduced by analog-transmitter components.

42. A predistortion circuit as claimed in claim 38 additionally comprising a programmable delay element coupled between said complex-forward-data-stream source and said feedback section, said programmable delay element being configured to produce a delayed-complex-forward-data stream from said complex-forward-data stream, said delayed-complex-forward-data stream being temporally aligned with said complex-return-data stream.

43. A predistortion circuit as claimed in claim 42 wherein:

said predistortion circuit additionally comprises a correlator having inputs coupled to said programmable delay element and to said feedback section and having an output coupled to said controller; and

said controller implements an estimation-and-convergence algorithm through said correlator in order to bring said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream.

44. A predistortion circuit as claimed in claim 38 wherein:

said one or more estimation-and-convergence algorithms are responsive to said complex-forward-data stream and to said complex-return-data stream;

said complex-forward-data stream and said complex-return-data stream exhibit forward-error and return-error levels, respectively, with said return-error level being greater than said forward-error level; and

said one or more estimation-and-convergence algorithms are configured to transform increased algorithmic processing time into reduced effective-error level for said complex-return-data stream.

45. A method of digitally compensating for linear distortion introduced by analog-transmitter components of a digital communications transmitter, said method comprising:

quadrature-balancing a complex-forward-data stream in response to quadrature balance parameters to generate a balanced-complex-forward-data stream;

providing said balanced-complex-forward-data stream to said analog-transmitter components;

at said transmitter, down-converting a feedback signal obtained from said analog-transmitter components to generate a complex-return-data stream; and

processing said complex-return-data stream at said transmitter to generate said quadrature balance parameters.

46. A method as claimed in claim 45 wherein:

said quadrature-balancing activity is performed by an equalizer section; and

said processing activity compensates for frequency dependent quadrature gain and phase imbalance introduced by said analog-transmitter components.

47. A method as claimed in claim 46 wherein:

said equalizer section includes a non-adaptive equalizer and an adaptation engine; and

said quadrature-balancing activity comprises coupling said adaptation engine to said non-adaptive equalizer in response to said processing activity so that said adaptation engine will converge upon filter coefficients, then programming said filter coefficients into said non-adaptive equalizer.

48. A method as claimed in claim 47 wherein:

said non-adaptive equalizer is a complex equalizer having first and second sets of filter coefficients;

said adaptation engine accommodates a partial complex equalizer; and

said processing activity causes said adaptation engine to identify said first set of filter coefficients, then after identifying said first set of filter coefficients to identify said second set of filter coefficients.

49. A method as claimed in claim 46 additionally comprising:

forming a delayed-complex-forward-data stream in temporal alignment with said complex-return-data stream;

forming an error signal by combining said delayed-complex-forward-data stream and said complex-return-data stream; and

implementing an estimation-and-convergence algorithm in said equalizer section that converges upon filter coefficients which minimize said error signal.

50. A method as claimed in claim 46 wherein said equalizer section includes a first equalizer configured to filter said complex-forward-data stream and produce said balanced-complex-forward-data stream and includes a second equalizer configured to filter said complex-return-data stream.

51. A method as claimed in claim 50 wherein:

said analog-transmitter components include a power amplifier which is driven by a power-amplifier-input signal and which produces a power-amplifier-output signal;

said feedback signal is a first feedback signal derived from said power-amplifier-input signal;

said method additionally comprises, after down-converting said first feedback signal, down-converting a second feedback signal derived from said power-amplifier-output signal to generate said complex-return-data stream; and

said processing activity causes said first equalizer to compensate for linear distortion in said power-amplifier-input signal in response to said first feedback signal, then causes said first equalizer to compensate for linear distortion in said power-amplifier-output signal in response to said second feedback signal.

52. A method as claimed in claim 51 wherein said processing activity, after adjusting said first equalizer to compensate for linear distortion in said power-amplifier-output signal, causes said second equalizer to compensate for linear distortion in said power-amplifier-output signal.

53. A method as claimed in claim 52 wherein:

said first equalizer increases correlation between said power-amplifier-output signal and a first signal responsive to said complex-forward-data stream and having a first bandwidth; and

said second equalizer increases correlation between said power-amplifier-output signal and a second signal responsive to said complex-forward-data stream having a second bandwidth wider than said first bandwidth.

54. A method as claimed in claim 45 wherein said down-converting activity is performed by a digital-subharmonic-sampling downconverter.

55. A method as claimed in claim 45 wherein said processing activity controls one or more estimation-and-convergence algorithms in order to generate said quadrature balance parameters.

56. A method as claimed in claim 55 wherein said one or more estimation-and-convergence algorithms are responsive to said complex-forward-data stream and to said complex-return-data stream;

said complex-forward-data stream and said complex-return-data stream exhibit forward-error and return-error levels, respectively, with said return-error level being greater than said forward-error level; and

said one or more estimation-and-convergence algorithms are configured to transform increased algorithmic processing time into reduced effective-error level for said complex-return-data stream.

57. A method as claimed in claim 45 wherein:

said processing activity controls a programmable delay element which delays said complex-forward-data stream to produce a delayed-complex-forward-data stream; and

said processing activity comprises delaying said delayed-complex-forward-data stream into temporal alignment with said complex-return-data stream.

58. A method as claimed in claim 57 wherein said delaying activity comprises:

delaying said complex-forward-data stream to compensate for common mode delay between said complex-forward-data and complex-return-data streams; and

delaying said complex-forward-data stream to compensate for differential mode delay.

59. A method as claimed in claim 57 additionally comprising forming an error signal by combining said delayed-complex-forward-data stream and said complex-return-data stream.

60. A method as claimed in claim 59 wherein:

said quadrature-balancing activity is performed by an equalizer section; and

said processing activity causes said equalizer section to generate said quadrature balance parameters in response to said error signal, said quadrature balance parameters being provided by filter coefficients.

61. A method as claimed in claim 45 wherein:

said analog-transmitter components include a band-pass filter driven by an upconverter, said band-pass filter inserting a band-pass-filter delay;

said method additionally comprises rotating the phase of one of said complex-forward-data and complex-return-data streams relative to the other to compensate for said band-pass-filter delay.

62. A method as claimed in claim 61 wherein:

said rotating activity occurs prior to said processing activity and generates an aligned-data stream; and

said processing activity processes said aligned-data stream.

63. A method as claimed in claim 45 wherein:

said analog-transmitter components include a power amplifier which is driven by a power-amplifier-input signal and which produces a power-amplifier-output signal;

said feedback signal is a first feedback signal derived from said power-amplifier-input signal; and

said method additionally comprises, after down-converting said first feedback signal, down-converting a second feedback signal derived from said power-amplifier-output signal to generate said complex-return-data stream.

64. A method as claimed in claim 45 wherein:

said quadrature-balancing activity is performed by an equalizer;

said processing activity generates filter coefficients for said equalizer, said filter coefficients serving as said quadrature balance parameters, and said filter coefficients causing said equalizer to compensate for linear distortion introduced by a portion of said analog-transmitter components upstream of a power amplifier; and

said processing activity comprises revising said filter coefficients after compensating for said linear distortion introduced by said portion of said analog-transmitter components upstream of said power amplifier to additionally compensate for linear distortion introduced by said power amplifier.

65. A method as claimed in claim 45 wherein:

said complex-return-data stream exhibits a lower resolution than is exhibited by said complex-forward-data stream and than is exhibited by said balanced-complex-forward-data stream.